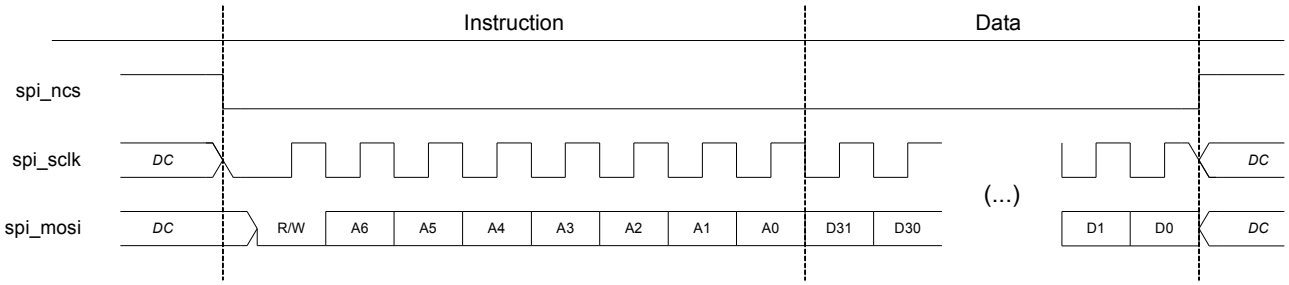
SPI configuration port

A write or read operation is initiated by pulling **spi_ncs** low. There are two parts to a communication cycle with the FPGA. In the first part, a 8-bit instruction word is written to the FPGA, coincident with the first 8 **spi_sclk** rising edges. The instruction word provides information regarding the data transfer, which is the second part of the communication cycle. The instruction word defines whether the upcoming data transfer is a read or a write and the starting register address for the first word of the data transfer.

7	6	5	4	3	2	1	0
R/$\overline{W}$	ADDR						

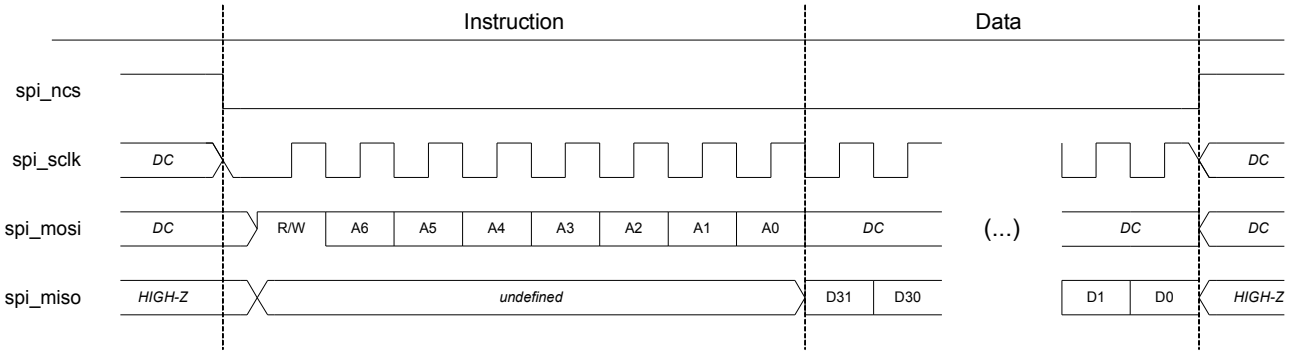
Setting a register value

If the instruction word is for a write operation, the next 32 **spi_sclk** cycles clock in data for the address specified in the instruction word. Data bits are registered on the rising edge of **spi_sclk**.



Reading a register value

If the instruction word is for a read operation, the next 32 SCLK cycles clock out the data from the address specified in the instruction word. The readback data is updated on the falling edge of **spi_sclk**.



Register set description

Register 0x00

Identification

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MAGIC															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAGIC															

MAGIC [31..0] R **Magic Identifier**

32 bit unsigned integer

The magic value can be used to detect is the FPGA is running and the communication interface is working. It always reads **0xDEADBEEF** at the moment.

Register 0x01

PWM #1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DUTY															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FREQ															

FREQ [15..0] R/W **PWM1 Frequency**

16 bit unsigned integer

The frequency of the first PWM output is configured vis this value:

$$PWM_{freq} = \left(\frac{80\,MHz}{FREQ + 1} \right)$$

DUTY [31..0] R/W **PWM1 Duty Cycle**

16 bit unsigned integer

The duty cycle of the first PWM output is configured vis this value:

$$PWM_{duty} = \left(\frac{DUTY}{FREQ + 1} \right)$$

Register 0x02

PWM #2

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DUTY															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FREQ															

FREQ [15..0] R/W **PWM1 Frequency**

16 bit unsigned integer

The frequency of the second PWM output is configured vis this value:

$$PWM_{freq} = \left(\frac{80\,MHz}{FREQ + 1} \right)$$

DUTY [31..0] R/W **PWM1 Duty Cycle**

16 bit unsigned integer

The duty cycle of the second PWM output is configured vis this value:

$$PWM_{duty} = \left(\frac{DUTY}{FREQ + 1} \right)$$

Register 0x03

ADC Timing

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACQLEN								**CLKDIV**							

CLKDIV [7..0] R/W **AD7357 SCK Frequency**

8 bit unsigned integer

The frequency of the SCK line to the AD7357 ADC is configured via this value:

$$F_{SCK} = \left(\frac{80\,MHz}{CLKDIV} \right)$$

DUTY [15..8] R/W **AD7357 Acquisition Time**

8 bit unsigned integer

Number of SCK cycles the CS Line to the AD7357 is held high between two conversions.

Register 0x04

SSC Interface

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLKDIV															**TM**

TM [0] R/W **Testmode**

Decides if the testmode of the SSC Interface is enabled:

- **0** normal operation
- **1** testmode enabled, data is replaced by a 16 bit counter

CLKDIV [15..8] R/W **SSC Clock Frequency**

8 bit unsigned integer

The frequency of the Clock line of the SSC interface to the MCU is configured via this value:

$$F_{SSC} = \left(\frac{80\,MHz}{2 \cdot (CLKDIV + 1)} \right)$$

Register 0x05

ADC Values

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
		ADC_Q													
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		ADC_I													

ADC_I [13..0] R **ADC Value A (I-Channel)**

14 bit unsigned integer

This register contains the last value read from the AD7357 on the A channel of the ADC.

ADC_Q [29..16] R **ADC Value B (Q-Channel)**

14 bit unsigned integer

This register contains the last value read from the AD7357 on the B channel of the ADC.

Register 0x06

Decimation Filter

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
													RATE		

RATE [2..0] R/W **Decimation Factor**

Configures the decimation factor of the filter:

- **000** no decimation
- **001** Samplerate is reduced by factor **2**
- **010** Samplerate is reduced by factor **4**
- **011** Samplerate is reduced by factor **8**
- **100** Samplerate is reduced by factor **16**
- **101** Samplerate is reduced by factor **32**
- **110** Samplerate is reduced by factor **64**

Register 0x07

ADC Sample Offset

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OFF_Q															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OFF_I															

OFF_I [15..0] R/W **Offset (I-Channel)**

16 bit signed integer

The value off **OFF_I** is added to each sample read from the AD7357 on the A channel. Before the addition, the ADC sample is expanded to 16 Bits.

OFF_Q [31..0] R/W **Offset (Q-Channel)**

16 bit signed integer

The value off **OFF_Q** is added to each sample read from the AD7357 on the B channel. Before the addition, the ADC sample is expanded to 16 Bits.