

Introduction to the X.21 Interface

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Disclaimer

- I never used a CSPDN back in the day
- All information presented is from historical books / specs / articles
- My understanding might be incorrect; Corrections welcome!

X.21? What is that?

- bit-synchronous serial interface
- traditionally (1976 through 1980s) used by circuit-switched packet data networks
- later (1990s) also used by some ISDN devices
- later (1990s) also used by some carrier leased lines (typically 64kbps .. 2048kbps)
- main specification is ITU Technical Recommendation X.21 (hence its name)

Serial Interface

- bits are transmitted successively one after the other
- most people are familiar with PC serial ports (RS232)
- also, virtually any microcontroller or SoC has a serial interface, typically provided by built-in UART (Universal Asynchronous Receiver Transmitter).
- RS-232 is (in most of its incarnations), however *asynchronous*, while X.21 is *synchronous*

Synchronous Interface

- *synchronous* means that receiver and transmitter share a common clock
- bits are then transmitted one synchronous with that clock, usually 1 bit per clock cycle
- synchronous interfaces do not need start/stop bits, so they have higher user data throughput at same bps
- simple synchronous interfaces need separate wires for clock, in addition to data
- example for other synchronous serial interfaces: SPI, I2C
- sometimes, uC will have peripherals called USART for an UART that's extended also for synchronous communications

X.21 - Use Case

- like RS232, X.21 is specified to be used between a DCE and DTE
 - DTE Data Terminal Equipment (Serial Terminal, Computer, ...)
 - DCE Data Communications Equipment (Modem, DAG/DFG, ...)
- in classic Telco networks, DCE was provided by the telco, and DTE by the user
- so an interface like X.21 was the *user interface* of said network
- signal naming and directions are always from the point of view of the DTE

X.21 Logical Signals

Below is a list of the logical signals on the X.21 interface. There are multiple electrical/physical incarnations of these.

- T Transmit (DTE -> DCE)
- C Control (DTE -> DCE)
- R Receive (DTE <- DCE)
- I Indication (DTE <- DCE)
- S Signal Element Timing (DTE <- DCE)
- B Byte Timing (DTE <- DCE)

X.21 Logical Signals: DTE -> DCE

- T (Transmit)
 - Data transmitted by DTE (to DCE)
 - Used both during Call Setup and data-transfer phase
- C (Control)
 - Used to specify the meaning of the *Transmit* data
 - Is ON during the data-transfer phase
 - Is OFF or ON during the call setup phase

X.21 Logical Signals: DTE <- DCE

- R (Receive)
 - Data Received by DTE (from DCE)
 - Used both during Call Setup and data-transfer phase
- I (Indication)
 - Used to specify the meaning of the *Receive* data
 - Is ON during the data-transfer phase
 - Is OFF or ON during the call setup phase

X.21 Logical Signals: DTE <- DCE Clock

- S (Signal Element Timing)
 - provides clock for *Receive* and *Transmit* data
- B (Byte Timing)
 - optional signal, not clear who ever used it
 - if it is used, it indicates the alignment of 8-bit bytes within the bitstream
 - normally high, but low during last bit of each 8-bit byte

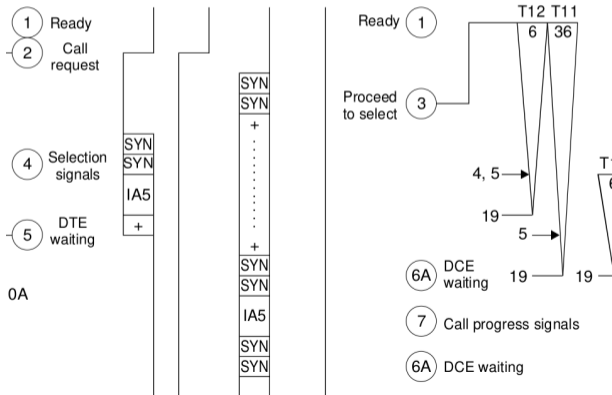
Clock signals are provided by the DCE to the DTE. The DCE will normally derive the clock from the telco network to ensure the user data is aligned with the (potentially higher order) synchronous multiplex of the network.

X.21 Call Setup Phase

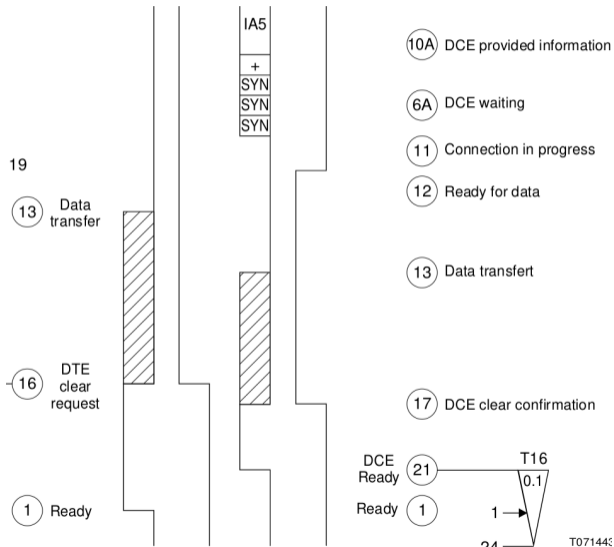
- Call signaling uses a reduced 7-bit-ASCII charset with odd parity bit
- Permitted characters are SYN, BEL "*" +, - ./" and 0-9
- Every message starts with *SYN*, *SYN* and ends with +
- Control + Indication signals play key role during call setup phase
- Call is released by dropping either Control (local release) or Indication (remote release)

X.21 Call Setup Phase

Calling and clearing DTE											
From DTE					From DCE						
State		T		C		R		I		State	
No.	Name	0	1	ON	OFF	0	1	ON	OFF	Name	No.



X.21 Call Setup Phase



X.21 Electrical Characteristics

X.27 + V.11 balanced differential signals (like RS-422/RS-485)

- permitted for any bit rate up to 10 Mbps.
- think of it as similar to RS-422 or RS-485

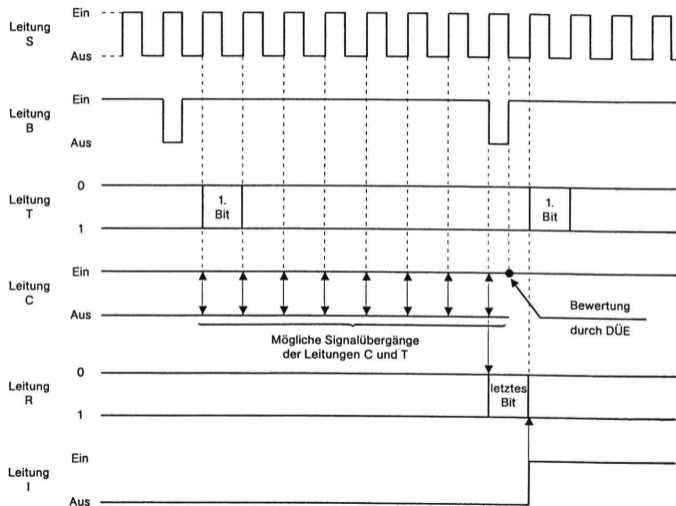
X.26 + V.10 unbalanced signals

- only permitted for bit rates of up to 9600 bps.
- think of it as similar to RS-232

We'll focus on the differential X/27/V.11 interface as we assume in practice it appears to be what most equipment uses. Some texts also claim that a DCE **always** is implemented in differential fashion, and only the DTE may use unbalanced at low bit rates.

X.21 Electrical + Timing

- two binary states signaled by voltage differential
- $U_a - U_b \leq -0.3V$: Logical Zero (Data) or ON (Control)
- $U_a - U_b \geq +0.3V$: Logical One (Data) or OFF (Control)
- Receive/Transmit Data edges are at rising clock edge
- Receive/Transmit Data is sampled at falling clock edge



X.21 Connector

- X.21 typically uses a 15-pin SUB-D connector
- DCE uses female
- DTE uses male

How to speak X.21 in 2023?

- Various line cards for older Cisco equipment (PA-8T-X21, WIC-1T, WIC-2T, HWIC-4T, HWIC-4A/S)
 - very inexpensive these days, even associated routers, and lots of them available
 - AFAICT, only support HDLC based network traffic, no support for call setup phase of CSPDNs
- (rare) Linux-supported X.21 PCI interface cards like FarSite FarSync T2U/T4U
 - if you can afford it, you can even buy new PCIe cards!
 - AFAICT, only support HDLC based network traffic, no support for call setup phase of CSPDNs



Not very satisfactory; Looks like we need to design a USB-attached DIY X.21 hardware adapter

OSHW DIY X.21 USB adapter plans

- should support the full/classic X.21 call set-up phase
- should support (switchable) DTE and DCE role
- should also be able to generate passive traces
- vogelchr (aka sigwinch) and I have been doing some early design/planning work for the electrical interace
- Not yet clear what kind of uC or FPGA will be used for USB interface side. RP2040? iCE40?
- Follow <https://osmocom.org/issues/5463> for updates

The End

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